Please consider new claim 21 as follows:

--21. (New) A system for forming a VLSI chip design comprising:

means for estimating signal routes between functional blocks;

means for determining resistance and capacitance values for the estimated signal routes; and

means for building a model of said signal routes including resistance and capacitance values.--

Remarks/Arguments

Applicants hereby traverse the outstanding rejections, and request reconsideration and withdrawal in light of the amendments and remarks contained herein. New claim 21 has been provided for consideration. Claims 1-21 are pending in this application.

A. Rejections under 35 U.S.C. § 112, second paragraph

Claims 1 is rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Specifically, the word "paths" in claim 1 lacks antecedent basis. In response, Applicants have amended claim 1 to change "paths" to "routes". Claims 7-8 have been amended for consistency with claim 1. Applicants have also amended claims 11, and 17-18 to correct a similar error. The claims have been amended only for the purpose of complying with the requirements of 35 U.S.C. § 112, second paragraph, and not for the purpose of narrowing their scope in the face of prior art. No new matter has been entered. As each element of indefiniteness cited by the Office Action has been addressed with a corresponding amendment, Applicants respectfully request the rejection of claim 1 under 35 U.S.C. § 112, second paragraph be withdrawn.

B. Rejection under 35 U.S.C. § 102(e)

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ho ('768).

It is well settled that to anticipate a claim, the reference must teach every element of the claim, see M.P.E.P. §2131. Moreover, in order for a prior art reference to be anticipatory

under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim," see M.P.E.P. § 2131, citing *In re Bond*, 15 US.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing Richardson v. Suzuki Motor Co., 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Applicants respectfully assert that the rejection does not satisfy these requirements.

Claim 1 defines a method for VLSI chip design that includes "estimating signal routes between functional blocks". Similarly, claim 11 defines a VLSI chip whose design was performed according to a method that includes "estimating signal routes between functional blocks". New claim 21 defines a system for forming a VLSI chip design that includes "means for estimating signal routes between functional blocks".

Ho, at least, does not disclose these limitations. More specifically, Ho does not estimate signal routes between functional blocks. Instead, Ho operates with already existing routes. Ho then maps the routes onto known geometries to compute the RC values. For example, as shown in FIGURE 2, the process flow gets the net (block 203), breaks polygons into smaller shapes (block 207), and then calculates the R values (block 209), and the C values block (211). This process does not involve the estimation of signal routes between functional blocks. Thus, Ho does not teach all of the claimed limitations. Therefore, the Applicants respectfully assert that for the above reasons claims 1 and 11, as well as new claim 21, are patentable over the 35 U.S.C. § 102 rejection of record.

Claims 2-10 and 12-20 depend directly from base claims 1 and 11, respectively, and thus inherit all limitations of their respective base claims. Each of claims 2-10 and 12-20 sets forth features and limitations not recited by Ho. Thus, the Applicants respectfully asserts that for the above reasons claims 2-10 and 12-20 are patentable over the 35 U.S.C. § 102 rejection of record.

Conclusion

For all the reasons given above, the Applicants submit that the pending claims distinguish over the prior art of record under 35 U.S.C. § 102, and meets the requirements of 35 U.S.C. § 112. Accordingly, the Applicants submit that this application is in full condition for allowance.

Applicants respectfully request that the Examiner call the below listed attorney if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

By: _____
Michael A. Papalas
Attorney/Agent for Applicant(s)
Reg. No. 40,381
Date: April 16, 2002
Telephone No. 214-855-8186

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: 4-16-2002

Typed Name: Joy H. Perigo

Signature: _____

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A method for VLSI chip design comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal [paths] routes including resistance and capacitance values.

7. (Amended) A method according to claim 4 wherein said step of estimating is performed based on input of signal [path] route configuration parameters.

8. (Amended) A method according to claim 7 wherein said signal [path] route configuration parameters specify one or more of signal [path] route material, physical size of signal [path] route material or spacing.

11. (Amended) A VLSI chip whose design was performed according to a method comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal [paths] routes including resistance and capacitance values.

17. (Amended) A VLSI chip according to claim 14 whose design was performed according to the method wherein said step of estimating is performed based on input of signal [path] route configuration parameters.

18. (Amended) A VLSI chip according to claim 17 whose design was performed according to the method wherein said signal [path] route configuration parameters specify one or more of signal [path] route material, physical size of signal [path] route material or spacing.

Please consider new claim 21 as follows:

--21. (New) A system for forming a VLSI chip design comprising:

means for estimating signal routes between functional blocks;

means for determining resistance and capacitance values for the estimated signal routes; and

means for building a model of said signal routes including resistance and capacitance values.--